IN THE CLAIMS

Please cancel claim 38.

Please add claims 44-45.

Please amend claims 22, 41, and 43 as follows:

1.-21. (Cancelled)

22. (Currently Amended) A vertically integrated field-effect transistor comprising:

a first electrically conductive layer;

a middle layer, formed partially from dielectric material, on the first electrically conductive layer;

a second electrically conductive layer on the middle layer; and

a nanostructure integrated in a via hole introduced into the middle layer, the nanostructure further comprising a first end portion that is coupled to the first electrically conductive layer and a second end portion that is coupled to the second electrically conductive layer;

wherein the first end portion of the nanostructure forms a first source/drain region and the second end portion of the nanostructure forms a second source/drain region of the field-effect transistor;

wherein the middle layer, between two adjacent dielectric sublayers, has a third electrically conductive layer, the thickness of which is less than the thickness of at least one of the dielectric sublayers; and

wherein a ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is formed from and arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein.

23. (Previously Presented) The field-effect transistor of claim 22, wherein catalyst material for catalyzing the formation of the nanostructure is arranged between the first conductive layer and the nanostructure.

24. (Previously Presented) The field-effect transistor of claim 23, wherein the third electrically conductive layer surrounds the nanostructure in a region around the first or second end portion.

25. (Previously Presented) The field-effect transistor of claim 24, wherein the thickness of the third electrically conductive layer is less than the thickness of both dielectric sublayers.

26. (Cancelled)

27. (Previously Presented) The field-effect transistor of claim 22, wherein the middle layer has an additional electrically conductive layer, which at least one additional electrically conductive layer serves as an additional gate electrode of the field-effect transistor, with an additional ring structure formed from an electrically insulating material as an additional gate-insulating region of the field-effect transistor being arranged along the via hole that has been introduced in the additional electrically conductive layer.

28. (Previously Presented) The field-effect transistor of claim 22, having an additional field-effect transistor above the field-effect transistor.

29. (Previously Presented) The field-effect transistor of claim 28, wherein the field-effect transistor and the additional field-effect transistor are connected to one another as an inverter circuit.

30. (Previously Presented) The field-effect transistor of claim 22, wherein the first and second electrically conductive layer includes one of a group comprising tantalum, tantalum nitride, titanium, molybdenum, aluminum, titanium nitride, and a ferromagnetic material.

31. (Previously Presented) The field-effect transistor of claims 27, wherein the third and additional electrically conductive layer comprises one of a group comprising polysilicon, tantalum, titanium, niobium, and aluminum.

32. (Previously Presented) The field-effect transistor of claim 22, wherein the dielectric material of the middle layer is one or a combination of the materials in a group comprising silicon dioxide, silicon nitride, and silicon dioxide doped with potassium ions.

33. (Previously Presented) The field-effect transistor of claim 22, wherein the nanostructure includes one of a group comprising a nanotube, a bundle of nanotubes, and a nanorod.

34. (Previously Presented) The field-effect transistor of claim 33, wherein the nanorod includes one of a group comprising silicon, germanium, indium phosphide, gallium nitride, gallium arsenide, zirconium oxide and a metal.

35. (Previously Presented) The field-effect transistor of claim 33, wherein the nanotube is one of a group comprising a carbon nanotube, a carbon-boron nanotube, a carbon-nitrogen nanotube, a tungsten sulfide nanotube, and a chalcogenide nanotube.

36. (Previously Presented) The field-effect transistor of claim 23, wherein the nanostructure is a carbon nanotube, and wherein the catalyst material is one of a group comprising iron, cobalt, and nickel.

37. (Previously Presented) The field-effect transistor of claim 23, wherein the nanostructure is a gallium arsenide nanorod, and wherein the catalyst material includes gold.

38. (Cancelled)

39. (Previously Presented) The field-effect transistor of claim 22, formed exclusively from dielectric material, metallic material and the material of the nanostructure.

40. (Previously Presented) The field-effect transistor of claim 22, formed on a substrate made from polycrystalline or amorphous material.

41. (Currently Amended) A field-effect transistor comprising:

a first conductive layer;

a middle layer on the first conductive layer, the middle layer having a via hole therein, and having a third conductive layer between two adjacent dielectric sublayers, the third electrically conductive layer forming the gate electrode of the field-effect transistor;

a second conductive layer on the middle layer;

a nanostructure integrated in the via hole and having a first source/drain region of the field-effect transistor that is coupled to the first conductive layer and a second source/drain region of the field-effect transistor that is coupled to the second conductive layer, and

ring-shaped means within the third electrically conductive layer of the middle layer along the via hole, for providing a gate-insulating region of the field-effect transistor, wherein the ring-shaped means is formed from the third electrically conductive layer.

42. (Previously Presented) The field-effect transistor of claim 41, wherein the thickness of the third conductive layer is less than the thickness of the dielectric sublayers.

43. (Currently Amended) A method for fabricating a vertically integrated field-effect

transistor, comprising:

forming a first electrically conductive layer;

forming a middle layer partially from dielectric material;

introducing a via hole into the middle layer;

forming a nanostructure having a first end portion and a second end portion in the via hole, the first end portion being coupled to the first electrically conductive layer, and the first end portion of the nanostructure forming a first source/drain region and the second end portion of the nanostructure forming a second source/drain region of the field-effect transistor;

forming a second electrically conductive layer on the middle layer and coupling the second electrically conductive layer to the second end portion of the nanostructure; and

forming the middle layer in such a manner that a third electrically conductive layer is formed between two adjacent dielectric sublayers, the thickness of which third electrically conductive layer is less than the thickness of at least one of the dielectric sublayers, wherein a ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is formed from and arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein.

44. (New) A vertically integrated field-effect transistor comprising:

a first electrically conductive layer;

a middle layer, formed partially from dielectric material, on the first electrically conductive layer;

a second electrically conductive layer on the middle layer; and

a nanostructure integrated in a via hole introduced into the middle layer, the nanostructure further comprising a first end portion that is coupled to the first electrically conductive layer and a second end portion that is coupled to the second electrically conductive layer;

wherein the first end portion of the nanostructure forms a first source/drain region and the second end portion of the nanostructure forms a second source/drain region of the field-effect transistor;

wherein the middle layer, between two adjacent dielectric sublayers, has a third electrically conductive layer, the thickness of which is less than the thickness of at least one of the dielectric sublayers; and

wherein a ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein,

wherein the middle layer has an additional electrically conductive layer, which at least one additional electrically conductive layer serves as an additional gate electrode of the field-effect transistor, with an additional ring structure formed from an electrically insulating material as an additional gate-insulating region of the field-effect transistor being arranged along the via hole that has been introduced in the additional electrically conductive layer.

45. (New) A method for fabricating a vertically integrated field-effect transistor, comprising:

forming a first electrically conductive layer;

forming a middle layer partially from dielectric material;

introducing a via hole into the middle layer;

forming a nanostructure having a first end portion and a second end portion in the via hole, the first end portion being coupled to the first electrically conductive layer, and the first end portion of the nanostructure forming a first source/drain region and the second end portion of the nanostructure forming a second source/drain region of the field-effect transistor;

forming a second electrically conductive layer on the middle layer and coupling the second electrically conductive layer to the second end portion of the nanostructure; and

forming the middle layer in such a manner that a third electrically conductive layer is formed between two adjacent dielectric sublayers, the thickness of which third electrically conductive layer is less than the thickness of at least one of the dielectric sublayers, wherein a ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein, and

forming the middle layer in such a manner that it has an additional electrically conductive layer, which at least one additional electrically conductive layer serves as an additional gate electrode of the field-effect transistor, with an additional ring structure formed from an electrically insulating material as an additional gate-insulating region of the field-effect transistor being arranged along the via hole that has been introduced in the additional electrically conductive layer.